Unchanged claim 3

3. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal.

Unchanged claim 4

4. The invention as defined in claim 1 wherein MOS transistor is a negative metal oxide semiconductor (NMOS) transistor.

Unchanged claim 5

5. The invention as defined in claim 1 wherein MOS transistor is a positive metal oxide semiconductor (PMOS) transistor.

Unchanged claim 6

6. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said power supply voltage supplied from said first power supply terminal is higher than a voltage supplied from said second power supply terminal.

Unchanged claim 7

7. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said power supply voltage supplied from said first power supply terminal is lower than a voltage supplied from said second power supply terminal.

Unchanged claim 8

8. The invention as defined in claim 1 wherein said MOS transistor is a negative metal oxide semiconductor (NMOS) transistor, said NMOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said first power supply terminal is the positive power supply terminal for said integrated circuit and said second power supply terminal is the negative power supply terminal for said integrated circuit.

Unchanged claim 9

9. The invention as defined in claim 1 wherein said MOS transistor is a positive metal oxide semiconductor (PMOS) transistor, said PMOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said first power supply terminal is the negative power supply terminal for said integrated circuit and said second power supply terminal is the positive power supply terminal for said integrated circuit.

Unchanged claim 10

10. The invention as defined in claim 1 wherein said voltage that is derived from said power supply voltage and has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage has a larger absolute value than said power supply by one threshold voltage of said MOS transistor.

Unchanged claim 11

11. The invention as defined in claim 1 wherein said voltage that is derived from said power supply voltage is generated from said power supply voltage by a high voltage generator.

Unchanged claim 12

12. The invention as defined in claim 1 further including on said integrated circuit a high voltage generator that generates said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

Unchanged claim 13

13. The invention as defined in claim 1 further including on said integrated circuit a high voltage generator that generates said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage, said high voltage generator comprising:

an oscillator generating an oscillating output signal;

a voltage doubler receiving as an input said oscillating output signal from said oscillator and supplying as an output a signal that has an average larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage;

a clamp which receives as an input said output of said voltage doubler and supplies an output voltage substantially clamped to a prescribed value that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage;

and a ripple filter which filters said output of said clamp and supplies the output of said high voltage generator, which said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

Replacement claim 14

14. (Amended) An active inductor on an integrated circuit, comprising:

a metal oxide semiconductor (MOS) transistor; and

a beyond voltage generator which generates a beyond voltage that is either greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

wherein said MOS transistor is coupled to said beyond voltage generator so as to bias said MOS transistor with said beyond voltage and so that said MOS transistor operates as said active inductor.

Replacement claim 15

15. (Amended) The invention as defined in claim 14 wherein said beyond voltage generator comprises:

an oscillator generating an oscillating output signal;

a voltage doubler receiving as an input said oscillating output signal from said oscillator and supplying as an output a voltage signal that has an average voltage that is either greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

a clamp which receives as an input said output of said voltage doubler and supplies an output voltage substantially clamped to a prescribed value that is outside the range of volta greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

and a ripple filter which filters said output of said clamp and supplies the output of said beyond voltage generator.

Replacement claim 16

16. (Amended) An active inductor on an integrated circuit, said active inductor comprising a metal oxide semiconductor (MOS) transistor that operates as said active inductor and being characterized in that said active inductor is biased using a voltage generated on said integrated circuit that is outside the range of the voltage supplied by a power supply for operating said integrated circuit.

Unchanged claim 17

17. The invention as defined in claim 16 wherein said MOS transistor is a negative metal oxide semiconductor (NMOS) transistor.

Unchanged claim 18

18. The invention as defined in claim 16 wherein said MOS transistor is a positive metal oxide semiconductor (PMOS) transistor.

Unchanged claim 19

19. The invention as defined in claim 16 wherein said active inductor is biased by coupling a gate of said MOS transistor to said voltage generated on said integrated circuit that is beyond the range of the voltage supplied by a power supply for operating said integrated circuit via an impedance.